REMARKS

Claims 1-9, 12, 16, 21, 22, and 39-52 were examined, and rejected in the Office Action.

Herein, claims 1-9, 16, 48 and 49 are cancelled. Claim 39 is amended to correct a typographical error.

It is requested that the Examiner consider the arguments below in view of the above amendments and allow the application.

A. Objection to the Drawings and Rejection under 35 U.S.C. 112

The Examiner objected to the drawings as not showing features claimed in claim 1, i.e., "an insulator covering the entire first surface of the second semiconductor chip," and "wherein the insulator is coupled between the adhesive layer and the first surface of the second semiconductor chip." Since this claim language appeared only in claim 1, cancellation of claim 1 should resolve this objection.

In response to the rejection of claims 21 and 39 under 35 U.S.C. 112, second paragraph, it is submitted that these claims are well supported in the specification and drawings.

Regarding claim 21, below is an annotated version of claim 21, wherein reference numbers from the exemplary embodiment of Figure 1 are inserted into the claim.

> 21. (Previously Amended) A semiconductor package (11) comprising:
> a first semiconductor chip (1) having opposed first (1a) and second (1b) surfaces, the second surface including a plurality of pads (1c);
> an adhesive layer (3) coupled to the second surface (1b) of the first semiconductor chip (1); and
> a second semiconductor chip (2) stacked over the second surface (1b) of the first semiconductor chip (1) and having opposed first (2a) and second (2b) surfaces; and
> an insulator (4) coupled to the first surface (2a) of the second semiconductor chip (2),
> wherein the insulator (4) is coupled between the first surface (2a) of the second semiconductor chip

(2) and the adhesive layer (3), and is between the first surface (2a) of the second semiconductor chip (2) and each of the pads (1c) of the second surface (1b) of the first semiconductor chip (1).

Claim 21's recitation of an insulator "between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip" clearly is shown in the example of Figure 1. In particular, the exemplary insulator 4 is overlying the bond pads 1c, and hence is "between" the bond pads 1c and the lower surface 2a of the upper semiconductor chip 2. Accordingly, the rejection of claim 21 under 35 U.S.C. 112 should be withdrawn, because the claim is completely understandable in view of Figure 1. Note that the placement of the insulator 4 over the bond pads 1c enables the feature that "the first conductive wires 5 do not directly contact to the first surface 2a of the second semiconductor chip 2." (Page 7, line 22 et seq.)

Regarding claim 39, below is an annotated version of claim 39, wherein reference numbers from the exemplary embodiment of Figure 1 are inserted into the claim.

39. (Previously Amended) A semiconductor package (11) comprising:
a substrate (7);
a first semiconductor chip (1) coupled to the substrate (7), the first semiconductor chip (1) having opposed first (1a) and second (1b) surfaces;
a second semiconductor chip (2) having opposed first (2a) and second (2b) surfaces;
a first means (3) coupled to the second surface (1b) of the first semiconductor chip (1) for coupling the first semiconductor chip (1) to the second semiconductor chip (2) in a stack;
at least one pad (1c) formed on the second surface (1b) of the first semiconductor chip (1); and
at least one first conductive wire (5) connecting the at least one pad (1c) of the first semiconductor chip (1) and the substrate(7);

at least one pad (2c) formed on the second surface (2b) of the second semiconductor chip (2);

at least one second conductive wire (6) connecting the at least one pad (2C) of the second semiconductor chip (2)and the substrate (7); and

an insulator (4) coupled between the first surface (2a) of the second semiconductor chip (2) and the first means (3), and overlying both the first means (3) and the at least one first conductive wire (5).

Claim 39's recitation of "an insulator coupled between the first surface of the second semiconductor chip and the first means, and overlying both the first means and the at least one first conductive wire" clearly is shown in Figure 1. The exemplary insulator 4 is coupled between the adhesive layer 3 and first surface 2a of the second semiconductor chip, and also is directly over both the adhesive layer 3 and the first conductive wires 5. In fact, in the example of Fig. 1, the conductive wires 5 contact the overlying portions of insulator 4, as is shown clearly in Figs. 1A and 1B. Accordingly, the rejection of claim 39 under 35 U.S.C. 112 should be withdrawn, because the claim is completely understandable in view of the figures.

Accordingly, it is submitted that no amendments to the drawings are necessary, and that claims 21 and 39 are allowable with respect to 35 U.S.C. 112, second paragraph.

B. Rejection of Claims 50-52 under 35 U.S.C. 102(e)

Claims 50-52 were rejected under 35 U.S.C. 102(e) as anticipated by Pai et al. The rejections are respectfully traversed.

Regarding claim 50, Pai et al. lack claim 50's feature of "an insulator coupled to the first surface of the second semiconductor chip, said insulator *being between each of the conductive wires and the first surface of the second semiconductor chip.*" Pai et al.'s film adhesive layer 166 is coupled to the lower surface of the upper semiconductor chip 130, but is entirely inward of the bonding wires 150 that are coupled to the lower semiconductor chip 110. Accordingly, because Pai et al. lack an insulator "between each of the bond wires and the first surface of the second semiconductor chip," the rejection of claim 50 must be withdrawn.

Regarding claim 51, Pai et al. lack claim 51's feature of "an insulator coupled to the first surface of the second semiconductor chip, said insulator *being between the pads of the second surface of the first semiconductor chip and the first surface of the second semiconductor chip.*" Pai et al.'s film adhesive layer 166 is coupled to the lower surface of the upper semiconductor chip 130, but is entirely inward of the bond pads of the lower semiconductor chip 110. Accordingly, since Pai et al. lack the feature of an insulator "between the pads of the second surface of the first semiconductor chip and the first surface of the second semiconductor chip, the rejection of claim 51 must be withdrawn.

C. Rejection of Claims under 35 U.S.C. 103

Claims 1-3, 5, 7-9, 12, 21, 22, and 39-49 were rejected under 35 U.S.C. 103 over Pai et al. Herein, claims 1-3, 5, 7-9, 48, and 49 are cancelled, rendering the objection moot.

It is respectfully submitted that claims 21 and 39 distinguish Pai et al., and hence the rejection of those claims and their respective dependent claims is respectfully traversed.

In particular, claim 21's feature of "an insulator" coupled "between the first surface of the between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip" is not shown in U.S. Patent 6,503,776 to Pai et al., because Pai et al.'s adhesive layer 162, dummy chip 160, and film adhesive 166 are entirely inward of the bonding pads of the semiconductor chip 110. Pai et al. show nothing in their Fig. 8 between the bonding pads of the semiconductor chip 110 and the lower surface of the upper semiconductor chip 130. Accordingly, claim 21 should be allowed.

Claim 39 also distinguishes Pai et al., because Pai et al.'s adhesive layer 162, dummy chip 160, and film adhesive 166 do not overlie the bond wires 150 coupled to the bonding pads of the lower semiconductor chip 110. Accordingly, Pai et al. lack claim 39's feature of "an insulator overlying both the first means and the at least one first conductive wire."

Since claims 21 and 39 distinguish Pai et al., these claims should be allowed, along with their respective dependent claims.

If there are any questions, please telephone the undersigned at (408) 451-5906 to expedite prosecution of this case.

Please especially call the undersigned if the Examiner wishes to discuss an amendment that might render the claims allowable, or if the Examiner is considering maintaining the

rejections rather than issuing a Notice of Allowance.

Respectfully submitted,

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I hereby certify that this correspondence is being sent by facsimile to 703 872 9306 on June 16, 2004

6-16-04 Carrie Peddick
Date Signature